XA-9673A
PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:

Hiroyuki MIZUNO et al.

Appln. No.

Filed: Herewith

For: SEMICONDUCTOR DEVICE

* * *

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Applicants wish to make of record the documents cited in prior Application No. 10/149,221 filed June 10, 2002, whether cited by Applicants or by the Patent Office. The documents are listed on the attached Form PTO-1449.

Respectfully submitted,

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January 6, 2004

FORM PTO-1449 LIST OF DOCUMENTS CITED BY APPLICANT	Atty. Docket No. XA-9673A	Appln. No.
	Applicant Hiroyuki MIZUNO et al.	
	Filing Date HEREWITH	Group

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Sub-class	Filing Date
	AA	4,973,864	11/90	Nogami	307	530	
	AB	5,854,562	12/98	Toyoshima et al.	327	55	
	AC	5,386,394	1/95	Kawahara et al.	365	208	
	AD	5,526,313	1/96	Etoh et al.	365	205	
	AE	5,457,657	10/95	Suh	365	205	
	AF	4,777,625	10/88	Sakui et al.	365	207	
	AG	5,274,598	12/93	Fujii et al.	365	205	
	AH	5,495,440	2/96	Asakura	365	149	
	AI	5,917,745	6/99	Fujii	365	63	
	AJ	5,978,255	11/99	Naritake	365	149	
	AK	5,995,403	11/99	Naritake	365	63	

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Examiner Initial		Document Number	Date	Country	Class	Sub-class	Translation
	AL	5-109272	4/30/93	JAPAN			abstract
	AM	64-1195	1/5/89	JAPAN			abstract
	AN						
	AO						
	AP						

OTHER (including author, title, date, pertinent pages, etc.)

	AQ	Lee, K-C., et al., "Low Voltage High Speed Circuit Designs for Giga-bit DRAMs", *1996 Symposium on VLSI Circuits Digest of Technical Papers*, 1996, pp. 104-105.
	AR	Itoh, Kiyoo, *VLSI Memory Design*, Baifukan, 1994, pp. 162-163.
	AS	

Examiner	Date Considered

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.